AMENDMENTS TO THE CLAIMS

Claim 1. (currently amended) Carrier recovery means - in particular in a channel decoding unit and/or a digital demodulating unit being particularly provided in a digital broadcasting receiver - for recovering a carrier of a received digital input signal, comprising at least first and second phase error detecting means ~~(2, 4)~~, in which:

~~–~~said first ~~or robust~~ phase error detecting means ~~(2)~~ is adapted for detecting a ~~first or~~ robust estimate for the phase error of the received digital input signal and for generating and~~/or~~ outputting a ~~first or~~ robust phase error signal ~~being~~ representative ~~for~~ of said robust phase error,

~~–~~said second ~~or frequency sensitive~~ phase error detecting means ~~(4)~~ is adapted for receiving ~~a~~ the robust phase error signal from said first phase error detecting means ~~(2) and in particular said first or robust phase error signal~~ and for deriving therefrom a ~~second or~~ frequency sensitive phase error signal which is representative of ~~at least for~~ the sign of the frequency error ~~or offset~~ with respect to the received digital input signal, and

~~–~~said ~~second or~~ frequency sensitive phase error signal is used to reduce the frequency error with respect to the received digital signal to enable locking to at least the carrier thereof.

Claim 2. (currently amended) Carrier recovery means according to claim 1, **characterized in** that said second phase error detecting means ~~(4)~~ comprises at least a subtracting / differentiating unit ~~(10)~~, a first limiting unit ~~(11)~~, and an adding / integrating unit ~~(12)~~ which are ~~in particular~~ connected in series ~~in that order~~.

Claim 3. (currently amended) Carrier recovery means according to claim 2, **characterized in** that said subtracting/differentiating unit ~~(10)~~ is adapted to receive ~~a phase error signal from said first phase error detecting means (2) and in particular~~ said ~~first or~~ robust phase error signal as an input signal and to generate and~~/or~~ output a ~~difference/~~differential signal ~~thereof~~.

Claim 4. (currently amended) Carrier recovery means according to claim 3, **characterized in** that said first limiting unit ~~(11)~~ is adapted to receive said ~~difference /~~ differential signal as an input signal and to generate and~~/or~~ output a limited signal ~~thereof~~ not exceeding given first lower and/or upper limits.

B1 Cont.

Claim 5. (currently amended) Carrier recovery means according to claim 4, **characterized in** that said adding/integrating unit ~~(12)~~ is adapted to receive said limited ~~difference /~~ differential signal as an input signal and~~/or~~ to generate and output a sum~~/integral~~ signal ~~thereof~~.

Claim 6. (currently amended) Carrier recovery means according to claim 5, **characterized in** that a second limiting unit ~~(13)~~ is provided which is ~~in particular~~ connected in series to said adding/integrating unit, ~~(12)~~ and

said second limiting unit ~~(13)~~ is adapted to receive said sum~~/integral~~ signal as an input signal and to generate and~~/or~~ output a limited signal ~~thereof~~ not exceeding given second lower and/or upper limits.

Claim 7. (currently amended) Carrier recovery means according to claim 1, **characterized in** that said first ~~or robust~~ phase error detecting means ~~(2)~~ is adapted to generate and~~/or~~ output a valid robust phase error signal of the received digital input signal when an amplitude of the received digital input signal is above a ~~given~~ first threshold, and

said second ~~or frequency sensitive~~ phase error detecting means ~~(4)~~ is adapted to use only said valid robust phase error signal as an input signal only for generating said ~~second or~~ frequency sensitive phase error signal.

Claim 8. (currently amended) Carrier recovery means according to claim 1, **characterized in** that lock detector means ~~(5)~~ is provided which is adapted to receive a phase error signal and to generate and~~/or~~ output a locking signal therefrom when said phase error signal and/or an average value thereof is beyond a ~~given~~ second threshold.

B1 Cont.

Claim 9. (currently amended) Carrier recovery means according to claim 8, **characterized in** that said locking detector means ~~(5)~~ is adapted to use said robust phase error signal and~~/or in particular~~ said valid robust phase error signal supplied by said first ~~or robust~~ phase error detecting means ~~(2)~~.

Claim 10. (canceled)

Claim 11. (new) A method of carrier recovery for recovering a carrier of a received digital input signal in a channel decoding unit or a digital demodulating unit of a digital broadcasting receiver, comprising the steps of:

detecting a robust estimate of the phase error for the received digital input signal;

generating and outputting a robust phase error signal representative of said robust phase error; and

deriving a frequency sensitive phase error signal from the robust phase error signal, said frequency sensitive phase error signal being representative of the sign of the frequency error with respect to the received digital input signal and being used to reduce the frequency error with respect to the received digital signal to enable locking to at least the carrier thereof.

B' Cont.

Claim 11 (new) The method according to claim 11, wherein said frequency sensitive phase error signal is detected by a second phase error detector comprising at least a subtracting / differentiating unit, a first limiting unit, and an adding / integrating unit which are connected in series.

Claim 12 (new) The method according to claim 12, wherein said subtracting / differentiating unit is adapted to receive said robust phase error signal as an input signal and to generate and output a differential signal.

Claim 13 (new) The method according to claim 13, wherein said first limiting unit is adapted to receive said differential signal as an input signal and to generate and output a limited signal not exceeding given first lower and/or upper limits.

Claim ~~15~~ 14. (new) The method according to claim 14, wherein said adding/integrating unit is adapted to receive said limited differential signal as an input signal and to generate and output a sum signal.

Claim ~~16~~ 15. (new) The method according to claim 15, wherein a second limiting unit is provided which is connected in series to said adding/integrating unit, and is adapted to receive said sum signal as an input signal and to generate and output a limited signal not exceeding given second lower and/or upper limits.

B1 cont.

Claim ~~17~~ 16. (new) The method according to claim 11, further comprising a step of generating and outputting a valid robust phase error signal of the received digital input signal when an amplitude of the received digital input signal is above a first threshold, and

generating said frequency sensitive phase error signal using only said valid robust phase error signal as an input signal.

Claim ~~18~~ 17. (new) The method according to claim 11, further comprising a step of generating and outputting a locking signal from a phase error signal when said phase error signal and/or an average value thereof is beyond a second threshold.

Claim ~~19~~ 18. (new) The method according to claim 18, wherein said locking signal is generated using said robust phase error signal and said valid robust phase error signal.